

FIG. 1 PRIOR ART

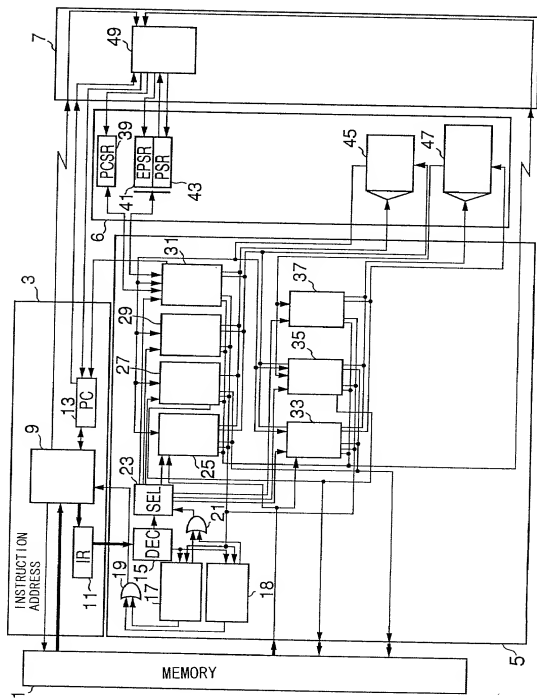


FIG. 2

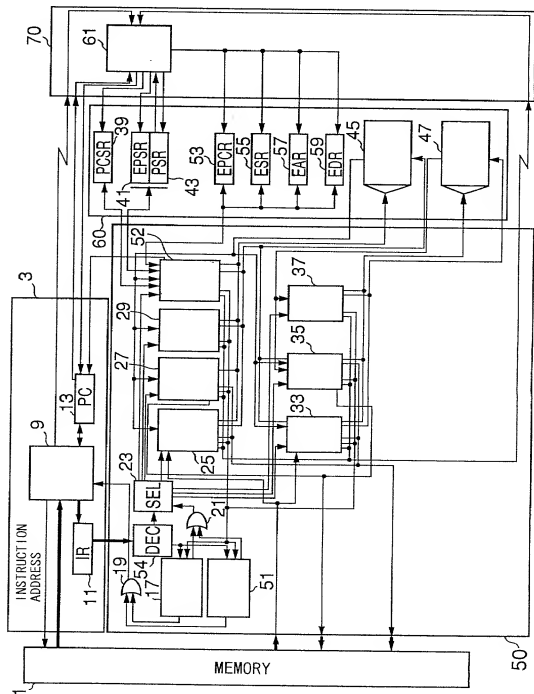


FIG.3

INSTRUCTION EXECUTION PART	KIND OF INSTRUCTION	EPCR	ESR	EAR	EDR
LOAD INSTRUCTION EXECUTION PART	LOAD INSTRUCTION	○	○	○	—
STORE INSTRUCTION EXECUTION PART	STORE INSTRUCTION	○	○	○	○
ARITHMETICAL INSTRUCTION EXECUTION PART	ARITHMETICAL INSTRUCTION	○	○		
FLOATING-POINT LOAD INSTRUCTION EXECUTION PART	FLOATING-POINT LOAD INSTRUCTION	○	○	○	—
FLOATING-POINT STORE INSTRUCTION EXECUTION PART	FLOATING-POINT STORE INSTRUCTION	○	○	○	○
FLOATING-POINT ARITHMETICAL INSTRUCTION EXECUTION PART	FLOATING-POINT ARITHMETICAL INSTRUCTION	○	○	—	—
OTHER INSTRUCTION EXECUTION PART	OTHER INSTRUCTION	○	○	—	—

1. Introduction



FIG.6

	6 th bit	5 th bit	4 th bit	Third bit	Second bit	First bit	0 th bit
—	ESR6	ESR5	ESR4	ESR3	ESR2	ESR1	ESR0

FIG.7

INSTRUCTION EXECUTION PART	KIND OF INSTRUCTION	EPCR0 ESR0	EPCR1 ESR1	EPCR2 ESR2	EPCR3 ESR3 EAR3	EPCR4 ESR4 EAR4	EPCR5 ESR5 EAR5 EDR5	EPCR6 ESR6 EAR6 EDR6
LOAD INSTRUCTION EXECUTION PART	LOAD INSTRUCTION				O			
STORE INSTRUCTION EXECUTION PART	STORE INSTRUCTION						O	
ARITHMETICAL INSTRUCTION EXECUTION PART	ARITHMETICAL INSTRUCTION	—	O	—	—	—	—	—
FLOATING-POINT LOAD INSTRUCTION EXECUTION PART	FLOATING-POINT LOAD INSTRUCTION					O		
FLOATING-POINT STORE INSTRUCTION EXECUTION PART	FLOATING-POINT STORE INSTRUCTION	—	—	—	—	—	—	O
FLOATING-POINT ARITHMETICAL INSTRUCTION EXECUTION PART	FLOATING-POINT ARITHMETICAL INSTRUCTION	—	—	O	—	—	—	—
OTHER INSTRUCTION EXECUTION PART	OTHER INSTRUCTION	O						

FIG.8

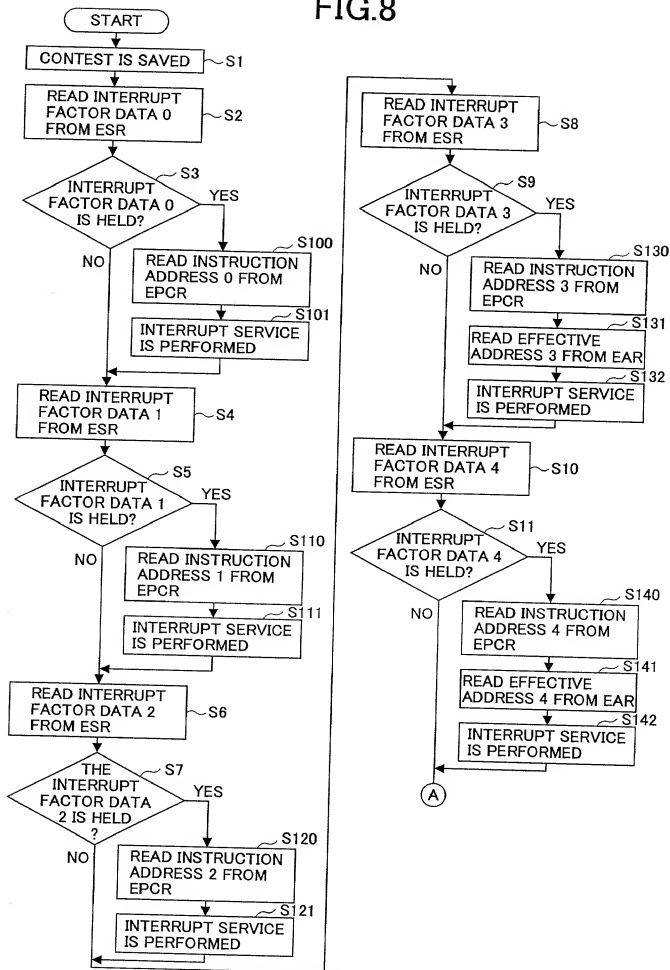


FIG.9

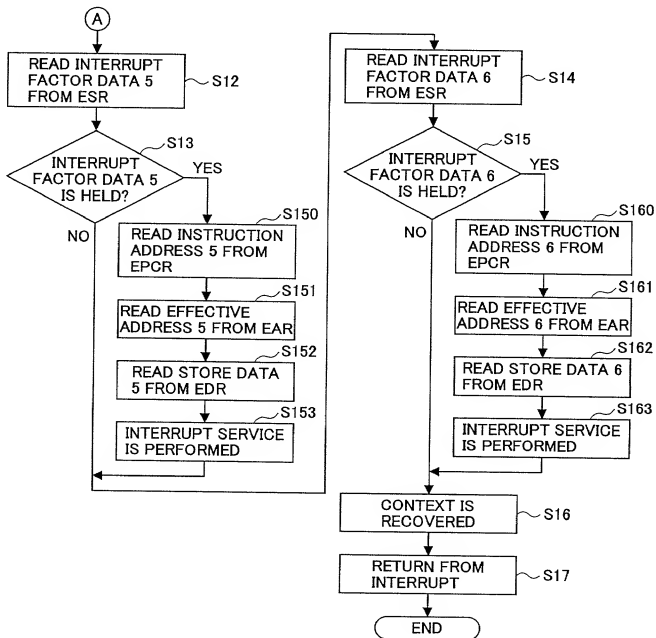


FIG.10

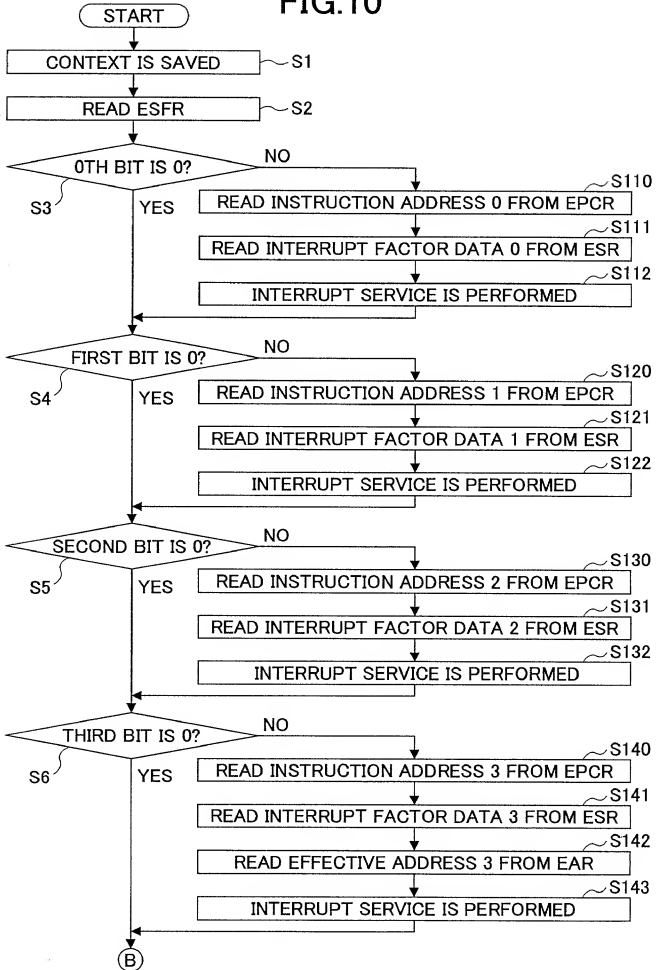


Figure 1. The structure of the proposed model.

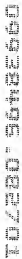


FIG. 12

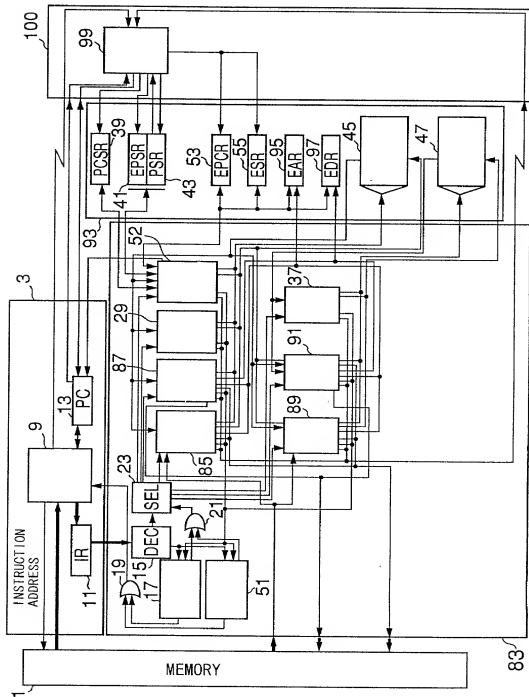


FIG. 13

